EEA
ÉLECTRONIQUE
ÉLECTROTECHNIQUE
ET AUTOMATIQUE
UNIVERSITÉ DE LYON

ÉCOLE DOCTORALE 160

Sujet de thèse

École doctorale EEA de Lyon

Merci de compléter l'ensemble des rubriques et de lire les notes de bas de page.

Etablissement d'inscription : Ecole Centrale de Lyon [1]
École doctorale : ED 160 EEA de Lyon dirigée par Mr Delachartre Philippe
Intitulé du doctorat : Electronique, Nanotechnologie, Optique et Laser [2]
Sujet de la thèse : Conception d'une fonction physiquement non-clonable basé sur les transistors à effet de champ ferroélectrique
Unité de recherche : INL[3], dirigée par Bruno Masenelli
Directeur/trice de thèse : Mr NAVARRO David
Co-directeur/trice de thèse (le cas échéant)[4] :
Co-directeur/trice de thèse en entreprise (le cas échéant) :

[1] A impérativement choisir dans la liste suivante : Ecole Centrale de Lyon, INSA de Lyon, Université Claude Bernard Lyon 1

[2] A impérativement choisir dans la liste suivante : Automatique // Electronique, Nanotechnologie, Optique et Laser // Génie Electrique // Ingénierie pour le vivant Traitement du signal et de l'Image)

[3] A impérativement choisir dans la liste suivante : Laboratoire Ampère, CITI, CREATIS, INL, LAGEP, LGEF

[4] Un/une co-encadrant-e n'est pas nécessairement co-directeur/trice de thèse puisque pour remplir ce rôle, il est nécessaire d'être habilité à diriger des recherches (pour plus de précision, voir le règlement intérieur de l'ED EEA, section 3.

Collaboration(s)/partenariat(s) extérieur(s) éventuels[5] :

Namlab, CEA, Laboratoire Hubert Curien, CEA

Domaine et contexte scientifiques :

Emerging technologies such as ferroelectric capacitors (FeCap) and transistors (FeFET, FemFET) are among the best technological options to overcome the bottleneck of classical computing architectures. Indeed, the main advantage of non-volatile emerging technologies lies in the possibility to change the computing paradigm, i.e. perform computing directly inside the memory or the computing unit's embedded memory. This allows a drastic reduction of data transfers thus increasing both the energy efficiency and the computation speed.

The promises in terms of energy and computing efficiency make these technologies extremely appealing for Internet of Things and embedded artificial intelligence applications. For both applications, high security level is mandatory to protect personal data and intellectual property of used devices. Physical Unclonable Functions (PUF) is today a hardware security primitive which can be used for both requirements. A PUF is a hardware unit capable of leveraging the manufacturing process variability that inevitably occurs during the fabrication of integrated circuit. In consequence, PUFs can be used to create a unique IC (Integrated Circuit) identifier of but also cryptographic keys under certain conditions.

Mots-clefs : Physical unclonable function, FeFET, FemFET, compact model, hardware security

Objectifs de la thèse :

The main objective of this thesis is to develop a new PUF based on Ferroelectric technologies and evaluate it according to the state of the art both in terms of quality and security attack.

In addition, PUF design are often close to True Random Number Generator (TRNG) because of noise extraction. Indeed, when a PUF try to extract static noise (manufacturing variations), TRNG extract random noise (electronic noise, thermal noise, jitter, …). Another objective of this thesis will be to study the possibility to create a dual PUF/TRNG structure.

Finally, the hardware security primitive will have to be tested and evaluated.

[5] Hors contrats doctoraux fléchés UMI par l'établissement, les sujets de thèse en cotutelle ne sont pas acceptés.

Verrous scientifiques :

- Playing with emerging technologies requires a fine understanding of their characteristics and manufacturing process. A first key point will be to integrate manufacturing variation inside the compact model of the ferroelectric devices in order to further study PUF design.

- A second challenge will be to find a simple circuit design allowing to extract the main process variation parameters efficiently.

- Designing such hardware primitive require more than just modelling and simulation. Indeed, to deeply evaluate the design, it is mandatory to manufacture a circuit that can be tested. This constitutes another challenge for the thesis.

Contributions originales attendues :

- A ferroelectric device compact model accounting for both static and random variations due to manufacturing process.

- An innovative PUF/TRNG design based on emerging ferroelectric devices

- An evaluation of the design based on simulation and on data collected on a manufactured circuit.

Programme de recherche et démarche scientifique proposée :

The works plan is defined as follow:

1st year. Bibliography and compact modelling of emerging ferroelectric devices

2nd year. PUF design and tape out submission for manufacturing process (or internal manufacture)

3rd year. Evaluation of PUF both at simulation and at circuit levels

Encadrement scientifique :

- **Description du comité d'encadrement :** [à compléter avec le rôle dans l'encadrement scientifique (en termes de compétences scientifiques, etc.) et le pourcentage d'implication du directeur de thèse [6] et des autres membres du comité[7]]

Nom Prénom	Labo / Equipe	Compétences scientifiques	Taux d'encadrement %
Mr NAVARRO David	INL Electronique	Low power electronic system	35
Mr MARCHAND Cédric	INL Electronique	Cryptographic function implementation and evaluation - PUF design and evaluation - FPGA and heterogeneous system design	35
Mr DELERUYELLE Damien	INL Electronique	Emerging memory technologies / device physics Compact modeling of FeRAM and FeFET devices	30

- Le comité d'évaluation de l'HCERES ayant demandé à l'école doctorale de limiter la taille du comité d'encadrement à deux membres (directeur de thèse compris), il est impératif de ne proposer des comités d'encadrement de taille plus importante que si cela est absolument nécessaire[8] et **de le justifier soigneusement.**

[6] Le directeur de thèse doit être un HdR rattaché à l'ED EEA ou en passe de le devenir avant juin de l'année en cours ou bénéficier d'une dérogation du Conseil Scientifique lors du dépôt du sujet de thèse.
[7] Dans le cas d'un comité d'encadrement réparti sur plusieurs établissements, la plus grande partie de l'encadrement est effectuée par des membres de l'établissement. Si l'encadrement de la thèse implique des membres hors de l'ED EEA, la part de l'encadrement des membres ED doit être très supérieur à 50%.
[8] Un certain nombre de commissions type CNU ne reconnaissent un co-encadrement qu'au-delà d'un certain pourcentage. Souvent l'encadrement est considéré comme effectif si > 30%.

Sujet de thèse à la frontière de plusieurs domaines, que les compétences des 3 encadrants recoupent.

- **Intégration au sein du (ou des) laboratoire(s)** (Département/Equipe(s) impliquée(s)) (**pourcentage du temps travail au sein de ce ou ces laboratoire(s)**) :

  INL / Electronique (100%)

Financement de la thèse : Contrat doctoral de l'établissement d'inscription

Profil du candidat recherché (prérequis) :

The candidate will have a strong background in topics related to the following area:

- Experience in micro-electronic circuit design and modelling.
- Software and languages under consideration of the computation, simulation, and hardware design: Cadence, VHDL, Verilog, C/C++, Python.
- Knowledge basic functions in hardware security (PUF, TRNG, …) will be also appreciated
- Knowledge in statistical evaluation will be appreciated
- The candidate should be curious, highly motivated, and flexible to address a highly inter-disciplinary project.
- Good English skills, writing and speaking, are needed.

Objectifs de valorisation des travaux de recherche :

All works done in the thesis will be valorized by publication in high level international conferences and journals.

Compétences qui seront développées au cours du doctorat :

During this PhD, the candidate will develop strong skills in compact modelling, variability analysis, microelectronic architecture design and evaluation.

Perspectives professionnelles après le doctorat :

The candidate will be able to apply for research and development positions in this topic, either in industry or in research labs.

Références bibliographiques sur le sujet de thèse :

Hardware security basic function and protection:

1. J. Guajardo, T. Guneysu, S. S. Kumar and C. Paar, "Secure IP-block distribution for hardware devices," 2009 IEEE International Workshop on Hardware-Oriented Security and Trust, 2009, pp. 82-89, doi: 10.1109/HST.2009.5224965.

2. C. Marchand, L. Bossuet, U. Mureddu, N. Bochard, A. Cherkaoui and V. Fischer, "Implementation and Characterization of a Physical Unclonable Function for IoT: A Case Study With the TERO-PUF," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 1, pp. 97-109, Jan. 2018, doi: 10.1109/TCAD.2017.2702607.

3. S. Sakhare and D. Sakhare, “A Review – Hardware Security Using PUF (Physical Unclonable Function)”, ICCCE 2019 (2020): 373-377, Springer, https://doi.org/10.1007/978-981-13-8715-9_45

4. A. Maiti, J. Casarona, L. McHale and P. Schaumont, "A large scale characterization of RO-PUF," 2010 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2010, pp. 94-99, doi: 10.1109/HST.2010.5513108.

5. McGrath, T., Bagci, I. E., Wang, Z. M., Roedig, U., & Young, R. J. (2019). “A puf taxonomy. Applied Physics Reviews”, 6(1), https://doi.org/10.1063/1.5079407.

6. J. -L. Danger et al., "Analysis of Mixed PUF-TRNG Circuit Based on SR-Latches in FD-SOI Technology," 2018 21st Euromicro Conference on Digital System Design (DSD), 2018, pp. 508-515, doi: 10.1109/DSD.2018.00090.

7. B. Gao, B. Lin, X. Li, J. Tang, H. Qian and H. Wu, "A Unified PUF and TRNG Design Based on 40-nm RRAM With High Entropy and Robustness for IoT Security," in IEEE Transactions on Electron Devices, vol. 69, no. 2, pp. 536-542, Feb. 2022, doi: 10.1109/TED.2021.3138365.

8. S. K. Satpathy et al., "An All-Digital Unified Physically Unclonable Function and True Random Number Generator Featuring Self-Calibrating Hierarchical Von Neumann Extraction in 14-nm Tri-gate CMOS," in IEEE Journal of Solid-State Circuits, vol. 54, no. 4, pp. 1074-1085, April 2019, doi: 10.1109/JSSC.2018.2886350.

Ferroelectric technology:

1. Yin X., Ni K., Reis D., Datta S., Niemier M. T. and Hu X. S., "An Ultra-Dense 2FeFET TCAM Design Based on a Multi-Domain FeFET Model," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 9, pp. 1577-1581, Sept. 2019. doi: 10.1109/TCSII.2018.2889225

2. I. O'Connor et al., "Prospects for energy-efficient edge computing with integrated HfO2-based ferroelectric devices," 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Verona, Italy, 2018, pp. 180-183. doi: 10.1109/VLSI-SoC.2018.8644809M

3. K. Ni, M. Jerry, J. A. Smith and S. Datta, "A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs," 2018 IEEE Symposium on VLSI Technology, 2018, pp. 131-132, doi: 10.1109/VLSIT.2018.8510622.

4. C. Li et al., "A Scalable Design of Multi-Bit Ferroelectric Content Addressable Memory for Data-Centric Computing," 2020 IEEE International Electron Devices Meeting (IEDM), 2020, pp. 29.3.1-29.3.4, doi: 10.1109/IEDM13553.2020.9372119.

5. H. Mulaosmanovic et al., "Evidence of single domain switching in hafnium oxide based FeFETs: Enabler for multi-level FeFET memory cells," 2015 IEEE International Electron Devices Meeting (IEDM), 2015, pp. 26.8.1-26.8.3, doi: 10.1109/IEDM.2015.7409777.

PUF with Ferroelectric technology:

1. S. Kim, K. Lee, M. -H. Oh, J. -H. Lee, B. -G. Park and D. Kwon, "Physical Unclonable Functions Using Ferroelectric Tunnel Junctions," in IEEE Electron Device Letters, vol. 42, no. 6, pp. 816-819, June 2021, doi: 10.1109/LED.2021.3075427.

2. S. Ramanujam and W. Burleson, "Reconfiguring the Mux-Based Arbiter PUF using FeFETs," 2021 22nd International Symposium on Quality Electronic Design (ISQED), 2021, pp. 257-262, doi: 10.1109/ISQED51717.2021.9424328.

3. X. Guo et al., "Exploiting FeFET Switching Stochasticity for Low-Power Reconfigurable Physical Unclonable Function," ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), 2021, pp. 119-122, doi: 10.1109/ESSCIRC53450.2021.9567880.