Call for applications – PhD candidate

Lyon Institute of Nanotechnology
Ecole Centrale de Lyon, 36 av. Guy de Collongue,
F-69134 Ecully, FRANCE
http://inl.cnrs.fr

PHOTONIC AUGMENTED SECURITY VIA PHYSICAL UNCLONABLE FUNCTIONS

Today, the exponential growth in the number of interconnected devices (75 billion IoT devices expected by 2025) demands for more robust and reliable security layers to guarantee hardware integrity and information security. Security layers are a fundamental part of our hardware and digital infrastructure fulfilling several key functions e.g., assuring that a hardware sub-system is not counterfeit or that a client has authentication rights onto a server. Counterfeiting poses a serious threat to the security of large-scale systems relying on the integration of several sub-systems e.g., counterfeit chips have been found in ballistic missiles and fighter jets. Besides, the daily exchange of sensitive data (medical data, banking information, etc.) requires that pitfalls shall not be exploited by an attacker to compromise the security of the platform e.g., recently discovered Meltdown and Spectre hardware vulnerabilities at the CPU level allow an attacker to access protected memory sectors e.g., storing passwords, secret keys…

The focus of this work will be to develop novel security layers that do not rely on the physical storage of a secret key in memory, potentially accessible exploiting SW or HW vulnerabilities. Physical unclonable functions (PUFs) represent a recent class of security layers that can be used to generate robust keys (responses) to given inputs (challenges) due to the complex character of their responses. Fabrication tolerances guarantee that each device cannot be cloned. Notwithstanding electronic PUFs are currently predominant, they are vulnerable to machine learning attacks. Conversely, photonic PUFs have demonstrated an increased strength against machine learning attacks due to their richer responses and larger number of physical quantities for key generation e.g., optical non-linearities.

In the framework of a research project funded by the French National Research Agency (ANR-PHASEPUF), the Heterogeneous Systems Design group at INL aims to develop novel silicon photonic PUFs for hardware integrity and information security. In this context we are currently looking for a (m/f) **PhD student** for a **3-year** contract.

Job description

This thesis aims to explore novel implementations of photonic PUFs based on CMOS-compatible Silicon Photonics approaches for applications in hardware integrity (identification) and information security (secure authentication).
This will involve (i) exploring various photonic architectures by means of system-level simulations considering the role of fabrication tolerances on the device modelling, (ii) assessing experimentally the performance of the prototypes (fabrication outsourced to CMOS foundries), (iii) carrying out an experimental analysis in terms of robustness and reliability by exploiting techniques well-known in the PUF and reliability communities, and (iv) proposing novel device/system designs and strategies to build more robust and reliable PUFs.

The work will involve behavioral and system-level modeling of photonic devices and architectures, robustness and reliability analysis of the designed architectures, and the proposal of novel design/system-level solutions.

Profile

You have or are about to obtain an MSc in Electronic or Physical Engineering / Computer Engineer / Computer Science with strong experience in at least one of the following areas: analog / digital / photonic integrated circuit design, multi-disciplinary or system-level modelling. Previous experience in characterization of photonic devices/systems is a plus. Excellent written and verbal communication skills in English. Fluency in French is also a plus, but not mandatory.

About INL

INL is a 250-strong research institute based in Lyon, France, carrying out fundamental and applied research in electronics, semiconductor materials, photonics and biotechnologies. The Heterogeneous Systems Design group is a leader in the area of advanced nanoelectronic design, with research projects and collaborations at both national and European level. Recent highlights include the development of high-performance design strategies for complex 3D integrated circuits, ferroelectric logic in memory, VNWFET-based logic and silicon photonic networks on chip.

Send CV and statement of purpose (in English or French) to

Fabio Pavanello / INL - Lyon Institute of Nanotechnology - Ecole Centrale Lyon – email: fabio.pavanello@ec-lyon.fr

Ian O'Connor / INL - Lyon Institute of Nanotechnology - Ecole Centrale Lyon – email: ian.oconnor@ec-lyon.fr