Energy Efficient Embedded Non-Volatile Memory & Logic Based on Ferroelectric Hf(Zr)O_2

3εFERRO is project for competitive, scalable FeRAM and logic-in-memory designs based on Si-compatible, ferroelectric $Hf_xZr_{1-x}O_2$. We report interface engineering, capacitor integration and FeFET logic design.

Energy efficiency

The 3εFERRO consortium is researching energy efficient non-volatile memory and logic devices based on Si-compatible ferroelectric $HfZrO_2$ (HZO) to provide advanced embedded solutions for normally-off microcontroller units used in IoT. The consortium is a balanced mix of large technology development laboratories and academia in partnership with ST Microelectronics to address the complex issues associated with materials optimization, circuit design, device fabrication and integration.

At A Glance

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EC Contribution: € **3.99**m

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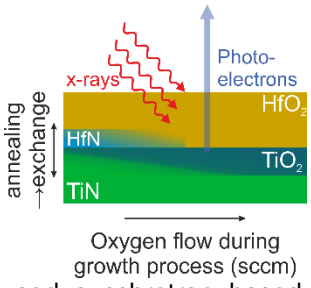
Appl. Phys. Lett. Special issue

As a result of the Covid-19 crisis, the high K workshop, organized by NaMLab and usually held in springtime, was cancelled. However, many contributions on ferroelectric hafnia and devices were already prepared. To ensure the broader scientific community benefits from the latest work, Applied Physics Letters is doing a Special Topic Edition for all planned speakers of the workshop. 41 contributions from the workshop participants are announced. The papers undergo the same peer-reviewing process as standard articles and are published as soon as accepted. The final version of the special issue comes out online in September. Here is the link.:

https://publishing.aip.org/publications/journals/special-topics/apl/ferroelectricity-in-hafnium-oxide-materials-and-devices/

Interface engineering HfO_2/TiN

Electrode/HZO interfaces may play an important role in the electrical performances of memory cells, influencing in particular imprint, retention and fatigue.



We have used synchrotron based hard X-ray photoelectron spectroscopy (HAXPES) to probe the interface chemistry and band line-up at both top and bottom interfaces.

The interface between the PVD grown HZO and the bottom TiN electrode was studied by the ForschunsZentrum Jülich team at the Petra-III synchrotron. They demonstrated the formation of a TiO_2-like layer. Importantly, the layer thickness can be engineered by varying the O_2 oxygen flow

during growth. The results have been submitted to *Advanced Electronic Materials*.

The CEA Saclay group has studied the electrode interfaces with the ALD grown HZO and demonstrated a chemical. The top interface forms an oxy-nitride layer whereas the bottom interface has a thicker Ti oxide which may be conducting. This work has been published in *Appl. Phys. Lett.*

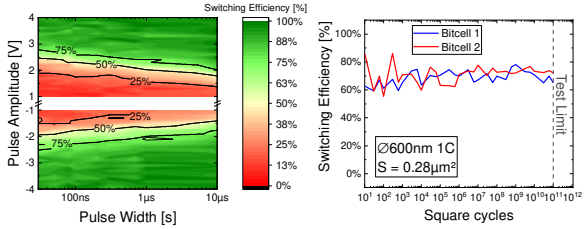
(https://doi.org/10.1063/5.0012595)

Successful co-integration of HZO scaled capacitors above 130 nm CMOS with excellent ferroelectric performances

During the last semester, in-depth electrical characterization was performed on the scaled HZO capacitors integrated between M4 and M5 of 130nm CMOS. We have demonstrated that despite the thermal budget imposed by BEOL integration, 10nm HZO films crystallize in the ferroelectric orthorhombic phase.

The remanent polarization 2.P_R measured on these BEOL-integrated scaled TiN/HZO/TiN capacitors (diameters from 600nm down to 300nm) reaches state-of-the-art values of 50 µC/cm², demonstrating that the shrink of the capacitor area has no detrimental impact on their performance.

Successful single cell operation was demonstrated on these capacitors, with switching speeds down to 30 ns and 2 V operating voltages, making HfO_2-based FeRAM technology very promising for low voltage low power applications.



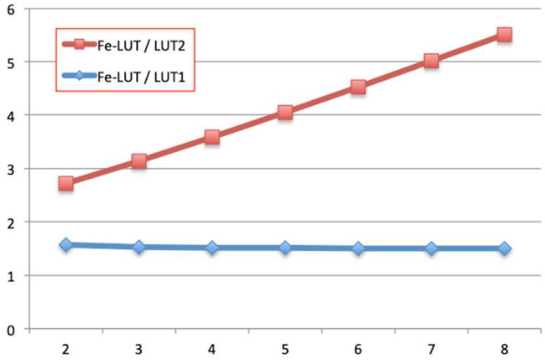
In addition, excellent endurance (> 10^{11} cycles) is reported on the capacitors, which is required for FeRAM devices for which the reading operation is destructive and necessitates a write-back. Finally, preliminary data retention measurements show no information loss after 24 hrs at 85°C.

The next step is to validate the excellent performance measured on single bitcells at the 16 kbit array level to derive distributions and demonstrate the full potential of this technology. A 16kbit 1T-1C FeRAM arrays with dedicated sense amplifier and write-back capability was designed and implemented on the new MAD200 test reticle. Results are expected early 2021.

Novel FeFET-based fine-grain Logic in Memory cells

In In the context of FeFET-based non-volatile logic design work coordinated by NaMLab and submitted to a GlobalFoundries run in April, ECL-INL implemented a novel ferroelectric Look-Up Table (LUT) and a Ternary content addressable and readable memory (TCAM-RAM).

The area- and energy-optimized LUT architecture merges a non-volatile storage element with the first multiplexer stage of the well-known Look up table (LUT) architecture. The resulting structure is a generic and scalable architecture for LUT of any size with a gain in terms of transistor count of 2^n transistors for an n-input LUT. In addition, the structure can activate only half of the storage elements when the configured function is evaluated, leading to energy savings. Finally, the ferroelectric LUT is non-volatile which means that powering off the device will not erase the configuration of the structure.



Fe-LUT improvement factor in overall transistor count compared to other FeFET-based LUTs, as a function of number of LUT inputs

The proposed TCAM-RAM structure overcomes multiple issues with conventional structures. Indeed, conventional TCAM architectures, based on classical field effect transistors, use a large number of devices and are most of the time volatile which means that the stored values must be written again each time the device is powered off. Using FeFETs, it is possible to design a 2-FeFET TCAM cell. However, state of the art TCAM architectures can only operate as content addressable memory and simply read a value stored at a specific address of the memory. ECL-INL's proposed structure solved this problem and enables content search by value (TCAM) and by address (RAM). For a 1-bit cell, the architecture requires just 3 transistors. The structure is scalable in order to achieve any word size

These new cells can be used in various contexts: embedded and reconfigurable devices (FPGAs, IoT, reconfigurable computing), fine-grain Logic in Memory, edge artificial intelligence, cryptographic functions, reversible computing.